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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/996,342	11/21/2001	Tohmas Eugene Waschura	WASC1821	1977

7590 10/01/2003

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EXAMINER
LAU, TUNG S

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 10/01/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/996,342	WASCHURA ET AL.	
	Examiner	Art Unit	
	Tung S Lau	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 September 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Deisch (U.S. Patent 6,072,340).

Regarding claim 1:

Deisch discloses an apparatus for measuring characteristics of a bit stream of binary pulses comprising control means for defining a window comparator (abstract, fig. 8), and logic means for accumulating event counts of the bit stream pulses falling within points inside the window comparator during durations of the binary pulse bit stream and drawing eye diagrams therefrom defining the bit stream characteristics (Col. 4, Lines 49-67, fig. 7, 8).

Regarding claim 7:

Deisch discloses apparatus for- measuring characteristics of a bit stream of binary pulses comprising control means for defining a window comparator of an array of columns and rows defining points for accumulating voltage counts of the binary pulse bit stream at time offsets during defined durations of the binary pulse bit stream (fig. 7, 8, Col. 2-3, Lines 40-7), and apparatus for creating a

voltage threshold window that moves between minimum and a maximum voltage levels (fig. 7) with each row of the array and for accumulating counts of voltage levels of the binary pulses occurring at the time offsets (fig. 10, unit 178) of the bit stream during a duration time when the pulse voltage levels are within the voltage threshold window at each row and column point of the array (fig. 7) and displaying the array column and row points of the accumulated time and voltage counts as an eye diagram defining characteristics of the bit stream of binary pulses (Col. 4, Lines 49-67, fig. 7, 8, 9g,10, 11a, 11b).

Regarding claim 8:

Deisch discloses apparatus for measuring characteristics of a bit stream of binary pulses including first control means for defining a window comparator of an array of columns and rows defining points for accumulating event counts at time offsets during defined duration times of the binary pulse bit stream (abstract, Col. 2-3, Lines 40-6), second control means for creating a voltage threshold window that moves between a minimum and maximum voltage threshold with each row of the array (fig. 7, graph Sout, St1) logic means (fig. 8, unit 100, 106) for detecting voltage levels of the binary pulses occurring at time offsets of the bit stream when the pulse voltage levels are within the voltage threshold at each row and column point of the array (fig. 8, unit 100), first counter means for accumulating counts of the detected binary pulse voltage levels at time offsets during each defined duration time of the binary pulse bit stream in a column and row point of

the array (fig. 7, 8), second counter means for determining duration of periods of the binary bit stream in which to accumulate the detected binary pulse voltage levels at each point of the array (fig. 5), and monitor apparatus for displaying the array column and row points of the accumulated event counts as an eye diagram defining characteristics of the bit stream of binary pulses (fig. 4, 5, 6).

Regarding claim 9:

Deisch discloses a method for determining characteristics of a bit stream of binary pulses comprising the steps of defining a window comparator (Col. 4, Lines 49-67) , and accumulating event counts of the bit stream pulses at time offsets during defined duration times of the binary pulse bit stream at points inside the window comparator and drawing an eye diagram therefrom defining the bit stream pulse characteristics (Col. 2-3, Lines 40-7, fig. 5, 6,7, 8).

Regarding claim 15:

Deisch discloses a method for determining characteristics of a bit stream of binary pulses comprising the steps of defining a window comparator of an array of columns and rows (fig. 7) defining points for accumulating event counts of the binary pulse bit stream at time offsets during defined durations of the binary pulse bit stream (Col. 2, Lines 40-6, fig. 8), creating a voltage threshold window that moves between a minimum voltage and a maximum at each row of the array (fig. 9g, 10), and accumulating counts of voltage levels of the binary pulses

occurring at time offses of the bit stream during a duration time when the pulse voltage levels (fig. 7) are within the voltage threshold window at each row and column point of the array and displaying the array column and row points of the accumulated event counts as an eye diagram defining characteristics of the bit stream of binary pulses (Col. 4, Lines 49-67, fig. 7).

Regarding claim 16:

Deisch discloses a method for determining characteristics of a bit stream of binary pulses comprising the steps of defining a window comparator of an array of columns and rows (fig. 7) defining points for accumulating event counts at time offsets during defined duration times of the binary pulse bit stream (Col. 2, Lines 40-67) , creating a voltage threshold window that moves between defined voltage levels at each row of the array, detecting voltage levels of the binary pulses occurring at the time of the bit stream when the pulse voltage levels are within the voltage threshold window at each row and column point of the array (fig. 7, 8), accumulating counts of the detected binary pulse voltage levels at the time offsets in a column and row point of the array (fig. 7), and displaying the array column and row points of the accumulated time and voltage counts as an eye diagram defining characteristics of the bit stream of binary pulses (fig. 9-10, 7, 8).

Regarding claims 2, 3, 4, 5 and 6:

Deisch discloses:

The apparatus for measuring characteristics of a bit stream of binary pulses wherein the control means comprises programmable means (fig. 8, unit 106, abstract) for establishing an array of columns and rows defining the points for accumulating counts of pulse voltage levels at time offsets during the duration times and for creating a voltage threshold window that moves between a minimum and maximum voltage with changes of rows of the array (fig. 7).

The apparatus for measuring characteristics of a bit stream of binary pulses wherein the logic means comprises logic circuitry for detecting voltage levels of the binary pulses occurring at various time offsets of the bit stream when the pulse voltage levels are within the voltage threshold window at each row and column point of the array (fig. 7, 8).

The apparatus for measuring characteristics of a bit stream of binary pulses wherein the logic means comprises first counter, second counter means for accumulating counts of the detected binary pulse voltage levels at the time offsets during each duration part of the binary pulse bit stream in a column and row point of the array (fig. 7, graph st1, st0).

The apparatus for measuring characteristics of a bit stream of binary pulses comprising apparatus for displaying the array column and row points of accumulated time and voltage counts as an eye diagram defining characteristics of the bit stream of binary pulses (fig. 7-9).

Regarding claims 10, 11, 12, 13 and 14:

Deisch discloses:

The method for determining characteristics of the bit stream of binary pulses wherein the window comparator defining step comprises the step of establishing an array of columns and rows defining the points for accumulating the event counts at time offsets during the defined duration times (fig. 7).

The method for determining characteristics of the bit stream of binary pulses wherein the window comparator defining step comprises the step of creating a voltage threshold window that moves with respect to a minimum and maximum voltage threshold wherein the voltage threshold window changes with respect to the rows of the array (fig. 7, point 53, 50).

The method for determining characteristics of the bit stream of binary pulses wherein the event count accumulating step comprises the step of detecting volltage levels of the binary pulses occurring at the time offsets of the bit stream when the pulse voltage levels are within the voltage threshold window at each row and column point of the array (fig. 7).

The method for determining characteristics of the bit stream of binary pulses wherein the event count accumulating step comprises the step of accumulating counts of the detected binary pulse voltage levels at the time offsets during each duration part of the binary pulse bit stream in a column and row point of the array (fig. 7).

The method for determining characteristics of the bit stream of binary pulses

wherein the event count accumulating step comprises the step of displaying the array column and row points of accumulated event counts as an eye diagram defining characteristics of the bit stream of binary pulses (fig. 7).

Response to Arguments

2. Applicant's arguments filed 9/2/2003 have been fully considered but they are not persuasive.

A. Applicant argues that the prior art does not show the 'control means for defining a windows comparator'; Deisch discloses 'control means for defining a windows comparator' in fig. 7, 8, 9, 12, unit 320, 305, Col. 2-3, Lines 40-7, Col. 4-5, Lines 49-46.

B. Applicant continues to argue that the prior art does not show ' discussion of any characteristic of a bit stream'; Deisch discloses ' discussion of any characteristic of a bit stream' in fig. 4, fig. 5, fig. 8, Col. 2-3, Lines 40-67, with the eye diagram and characteristic of the bit stream.

C. Applicant continues to argue that the prior art does not show ' discussion of any characteristic of a bit stream with an eye diagram'; Deisch discloses ' discussion of any characteristic of a bit stream with an eye diagram' in fig. 4, fig.

5, fig. 8, Col. 2-3, Lines 40-67, with the eye diagram and characteristic of the bit stream.

D. Applicant continues to argue that the prior art does not show 'logic means accumulation of event count of bit stream pulses'; Deisch discloses 'logic means accumulation of event count of bit stream pulses' in fig. 7, 8, 12, unit 320, Col. 2-3, Lines 40-67, with the eye diagram and characteristic of the bit stream.

E. Applicant continues to argue that the prior art does not show 'creating voltage threshold of any apparatus with maximum and minimum voltage comparator'; Deisch discloses 'creating voltage threshold of any apparatus with maximum and minimum voltage comparator' in fig. 4, 5, 6, 7, 8, 10, 12, unit 320, Col. 2-3, Lines 40-67, with the eye diagram and characteristic of the bit stream.

F. Applicant continues to argue that the prior art does not show 'counter means to detect accumulating counts of binary pulses'; Deisch discloses 'counter means to detect accumulating counts of binary pulses' in fig. 7, 8, unit 106, 108, 104, 122, fig. 9-11.

G. Applicant continues to argue that the prior art does not show 'display windows comparator with eye diagram'; Deisch discloses 'display windows comparator with eye diagram' in fig. 5, fig. 8, unit 122, fig. 10, unit 169.

H. Applicant continues to repeat the above arguments for the rest of the response, please refer points A-G for the response A.

Reminds to the applicant that while the meaning of claims of issued patents are interpreted in light of the specification, prosecution history, prior art and other claims, this is not the mode of claim interpretation to be applied during examination. During examination, the claims must be interpreted as broadly as their terms reasonably allowed. This means that the words of the claim must be given their plain meaning unless applicant has provided a clear definition in the specification. In re Zletz, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, EP 1143654 shows the system for measuring characteristics of a bit stream of binary pulses.

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tung S Lau whose telephone number is 703-305-3309. The examiner can normally be reached on M-F 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on 703-308-3126. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-5841 for regular communications and 703-308-5841 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

TC2800 RightFAX Telephone Numbers : TC2800 Official Before-Final RightFAX - (703) 872-9318, TC2800 Official After-Final RightFAX - (703) 872-9319

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